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EXAMINER

WALLING, MEAGAN S

ART UNIT	PAPER NUMBER
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2863

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 10/649,404	Applicant(s) GEDAMU ET AL.	
	Examiner Meagan S Walling	Art Unit 2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 August 2003.
 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) ☐ Claim(s) _____ is/are allowed.
 6) ☒ Claim(s) 1-3, 5, 7, 13-16 and 21 is/are rejected.
 7) ☒ Claim(s) 4, 6, 8-12 and 17-20 is/are objected to.
 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>8/26/03</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-3, 5, 7, 15, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable Kagami (US 5,394,369) in view of Lehmann et al. (US 2004/0140835).

Regarding claim 1, Kagami teaches test data corresponding to testing a plurality of semiconductor components, each one of the plurality of components residing on a different one of a plurality of semiconductor devices and each one of the components having a common location on the semiconductor device (see abstract); and a memory with logic configured to determine from the test data which of the plurality of components are defective components (column 3, lines 38-41), and further configured to specify on an output report the common location of the determined defective fuses when a number of the defective fuses are at least equal to a predefined portion to the plurality of components (see abstract).

Regarding claim 3, Kagami teaches that the semiconductor is on a wafer (column 3, line 25).

Regarding claim 7, Kagami teaches retrieving test data corresponding to test results from a plurality of semiconductor components, each one of the plurality of components residing on a different one of a plurality of semiconductor devices and each one of the components having a common location on the semiconductor device (see abstract); determining from the test data

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which of the plurality of components are defective components (column 3, lines 38-41); and specifying on an output report the common location of the determined defective fuses when a number of the defective fuses are at least equal to a predefined portion to the plurality of components (see abstract).

Regarding claim 15, Kagami teaches testing the plurality of components (see abstract).

Regarding claim 21, Kagami teaches receiving from memory test data corresponding to test results from a plurality of semiconductor components, each one of the plurality of components residing on a different one of a plurality of semiconductor devices and each one of the components having a common location on the semiconductor devices (see abstract); determining from the test data which of the plurality of components are defective components (column 3, lines 38-41); specifying on an output report the common location of the determined defective fuses when a number of the defective fuses are at least equal to a predefined portion to the plurality of components (see abstract).

Kagami does not teach that the semiconductor components are fuses (current claims 1, 7, 21).

Lehmann et al. teaches a fuse latch circuit to determine if a fuse is defective (see paragraph 3).

Regarding claim 2, Lehmann et al. teaches a fuse test device configured to test a plurality of fuses (see Ref. 200).

Regarding claim 5, Lehmann et al. teaches that the semiconductor device resides on an IC chip (see paragraph 84).

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It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Kagami and Lehmann et al. to determine if fuses are defective. The motivation for making this combination would be to save money by testing for defective fuses before the defective fuses cause overheating and to save time by checking the fuses all at one time.

2. Claims 13, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kagami in view of Lehmann et al. and further in view of Feinstein (US 6,701,003).

Regarding claim 16, Kagami teaches means for retrieving test data corresponding to test results from a plurality of semiconductor components, each one of the plurality of components residing on a different one of a plurality of semiconductor devices and each one of the components having a common location on the semiconductor device (see abstract); means for determining from the test data which of the plurality of components are defective components (column 3, lines 38-41); and means for specifying the common location of the determined defective fuses when a number of the defective fuses are at least equal to a predefined portion to the plurality of components (see abstract).

Kagami does not teach that the semiconductor components are fuses (current claim 16).

Lehmann et al. teaches a fuse latch circuit to determine if a fuse is defective (see paragraph 3).

It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Kagami and Lehmann et al. to determine if fuses are defective. The motivation for making this combination would be to save money by testing for defective fuses

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before the defective fuses cause overheating and to save time by checking the fuses all at one time.

Kagami and Lehmann et al. teach all of the limitations of claims 13, 14, and 16 except the limitations of displaying the output report (current claims 13 and 16) and printing the output report (current claim 14).

Feinstein teaches printing an error report showing defective components (column 5, lines 36-38).

It would have been obvious at the time of the invention to combine the teachings of Kagami and Lehmann et al. with the teachings of Feinstein to print the error report. The motivation for making this combination would be to have a record of errors to determine if a common error is being made and to correct that error.

Allowable Subject Matter

3. Claims 4, 6, 8-12, and 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for the indication of allowability of claim 4 is the inclusion of the limitation that the device comprises a fuse test unit configured to test the plurality of fuses when the semiconductor device resides on a die. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 6 is the inclusion of the limitation that the device comprises a fuse test unit configured to test the plurality of fuses when the semiconductor device resides on a circuit board. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 8 is the inclusion of the limitation of specifying the predefined portion as a percentage. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 9 and 17 is the inclusion of the limitation of retrieving the test data corresponding to the test results from a plurality of second fuses, each one of the plurality of second fuses residing on a different one of the semiconductor devices and each one of the plurality of second fuses having a second common location on the semiconductor devices; determining from the test data which of the plurality of second fuses are defective second fuses; and specifying on the output report the second common location of the determined defective second fuses when a number of the defective second fuses are at least equal to the predefined portion of the plurality of second fuses. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 10 and 18 is the inclusion of the limitation of retrieving the test data corresponding to the test results from a plurality of fuse arrays, each one of the fuse arrays having a plurality of array fuses and each one of the

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plurality of fuse arrays having a common fuse array location on the semiconductor devices', determining from the test data which of the plurality of array fuses are defective array fuses; and specifying on the output report the common fuse array location when a number of the defective array fuses are at least equal to a predefined portion of the array fuses. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 11 and 19 is the inclusion of the limitation of retrieving the test data corresponding to the test results from a plurality of fuse registers, each one of the fuse registers having a plurality of register fuses and each one of the plurality of fuse registers having a common fuse register location on the semiconductor devices', determining from the test data which of the plurality of register fuses are defective register fuses; and specifying on the output report the common fuse register location when a number of the defective register fuses are at least equal to a predefined portion of the register fuses. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 12 and 20 is the inclusion of the limitation of retrieving the test data corresponding to the test results from a grouping of fuses, each one of the grouped fuses in the grouping of fuses having a common location on the semiconductor devices; determining from the test data which of the grouped fuses are defective; and specifying on the output report the common location when a number of the defective grouped fuses are at least equal to a predefined portion of the grouped fuses. It is this limitation

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in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Meagan S Walling whose telephone number is (571) 272-2283. The examiner can normally be reached on Monday through Friday 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

msw


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